AMENDMENTS

Please amend the claims as follows:

1. (currently amended) An asynchronous pulse logic circuit comprising:

a first pulse generating component ~~(196)~~ for generating a sending pulse; and

a first converting component ~~(188)~~ for catching and holding said sending pulse and converting said sending pulses to a first level voltage connected to said first pulse generating component ~~(196)~~.

2. (currently amended) The asynchronous pulse logic circuit of claim 1, further comprising:

a second pulse generating component ~~(192)~~ for generating a resetting pulse;

a second converting component ~~(194)~~ for converting said resetting pulses to a second level voltage connected to said second pulse generating component ~~(192)~~;

a checking component ~~(190)~~ for ensuring no old output is still pending;

an N-input component ~~(199)~~ connected to said first pulse generating component ~~(196)~~; and

an N-output component ~~(198)~~ connected to said first converting component ~~(188)~~ whereby a STAPL left-right buffer ~~(186)~~ is formed.

3. (currently amended) The asynchronous pulse logic circuit of claim 1 further comprises:

a checking component ~~(190)~~ for ensuring no old output is still pending whereby said checking component ~~(190)~~ is connected to said first pulse generating component ~~(196)~~ and said first converting component ~~(188)~~ to form a first input-output block ~~(200)~~.

4. (original) The asynchronous pulse logic circuit of claim 3 further comprises:

a plurality of said input-output blocks.

5. (currently amended) The asynchronous pulse logic circuit of claim 4 further comprises:

an input-clearing block ~~(206)~~ comprising a second converting component ~~(194)~~ for converting pulses.

6. (currently amended) The asynchronous pulse logic circuit of claim 5 further comprises:

an acknowledgment block ~~(204)~~ comprising a second pulse generating component ~~(192)~~ for generating a resetting pulse.

7. (currently amended) The asynchronous pulse logic circuit of claim 6 further comprises:

a conditions block ~~(224)~~ whereby said second pulse generating component ~~(192)~~ is controlled by said conditions block ~~(224)~~ to conditionally reset each of said plurality of input-output blocks and input clearing block ~~(206)~~.

8. (currently amended) The asynchronous pulse logic circuit of claim 7 wherein said conditions block further comprises:

a third pulse generating component ~~(196)~~ for generating a sending pulse; and

a third converting component ~~(188)~~ for converting said sending pulses to said first level voltage connected to said third pulse generating component ~~(196).~~

9. (currently amended) The asynchronous pulse logic circuit of claim 1 wherein said first converting component ~~(188)~~ is modified to store states.

10. (currently amended) The asynchronous pulse logic circuit of claim 9 further comprises:

an updating component ~~(502)~~ comprising interlock component ~~(504)~~ wherein an updating pulse is generated to update the input state in said first pulse generating component ~~(196)~~, whereby a state-storing circuit ~~(234)~~ is formed.

11. (currently amended) The asynchronous pulse generating circuit of claim 1 further comprises:

an arbiter-filter ~~(239)~~; and

a checking component ~~(190)~~ for ensuring no old output is still pending whereby said checking component ~~(190)~~ and said arbiter-filter ~~(239)~~ are connected to said first pulse generating component ~~(196)~~ and said first converting component ~~(188)~~ to form a STAPL arbiter ~~(238).~~

12. (currently amended) The asynchronous pulse generating circuit of claim 11 wherein said first pulse generating component ~~(196)~~ generates a reset pulse for the input.

13. (currently amended) The asynchronous pulse generating circuit of claim 11 wherein said first pulse generating component ~~(196)~~ further comprises an interlock ~~(504)~~ component.

14. (currently amended) The asynchronous pulse generating circuit of claim 2 further comprises:

a QDI buffer ~~(240)~~ connected to said STAPL left-right buffer whereby an STAPL-to-QDI converter is formed.

15. (currently amended) The asynchronous pulse generating circuit of claim 2 further comprises:

a QDI buffer ~~(246)~~ connected to said STAPL left-right buffer whereby an QDI-to-STAPL converter is formed.

16. (new) An asynchronous pulse logic circuit comprising:

a first pulse generating component for generating a sending pulse;

a first converting component for converting pulses to a first level voltage connected to said first pulse generating component;

a second pulse generating component for generating a resetting pulse;

a second converting component for converting pulses to a second level voltage connected to said second pulse generating component;

a checking component for ensuring no old output is still pending;

an N-input component connected to said first pulse generating component; and

an N-output component connected to said first converting component whereby a STAPL left-right buffer is formed.

17. (new) The asynchronous pulse logic circuit of claim 16 further comprises:

a checking component for ensuring no old output is still pending whereby said checking component is connected to said first pulse generating component and said first converting component to form a first input-output block.

18. (new) The asynchronous pulse logic circuit of claim 17 further comprises:

a plurality of said input-output blocks.

19. (new) The asynchronous pulse logic circuit of claim 18 further comprises:

an input-clearing block comprising a second converting component for converting pulses.

20. (new) The asynchronous pulse logic circuit of claim 19 further comprises:

an acknowledgment block comprising a second pulse generating component for generating a resetting pulse.

21. (new) The asynchronous pulse logic circuit of claim 20 further comprises:

a conditions block whereby said second pulse generating component is controlled by said conditions block to conditionally reset each of said plurality of input-output blocks and input clearing block.

22. (new) The asynchronous pulse logic circuit of claim 21 wherein said conditions block further comprises:

a third pulse generating component for generating a sending pulse; and

a third converting component for converting pulses to said first level voltage connected to said third pulse generating component.

23. (new) An asynchronous pulse logic circuit comprising:

a first pulse generating component for generating a sending pulse;

a first converting component for converting pulses to a first level voltage connected to said first pulse generating component wherein said first converting component is modified to store states; and

an updating component comprising interlock component wherein an updating pulse is generated to update the input state in said first pulse generating component, whereby a state-storing circuit is formed.

24. (new) The asynchronous pulse generating circuit of claim 23 further comprises:

an arbiter-filter; and

a checking component for ensuring no old output is still pending whereby said checking component and said arbiter-filter are connected to said first pulse generating component and said first converting component to form a STAPL arbiter.

25. (new) The asynchronous pulse generating circuit of claim 24 wherein said first pulse generating component generates a reset pulse for the input.

26. (new) The asynchronous pulse generating circuit of claim 24 wherein said first pulse generating component further comprises an interlock component.

27. (new) The asynchronous pulse generating circuit of claim 16 further comprises:

a QDI buffer connected to said STAPL left-right buffer whereby an STAPL-to-QDI converter is formed.

28. (new) The asynchronous pulse generating circuit of claim 16 further comprises:

a QDI buffer connected to said STAPL left-right buffer whereby an QDI-to-STAPL converter is formed.